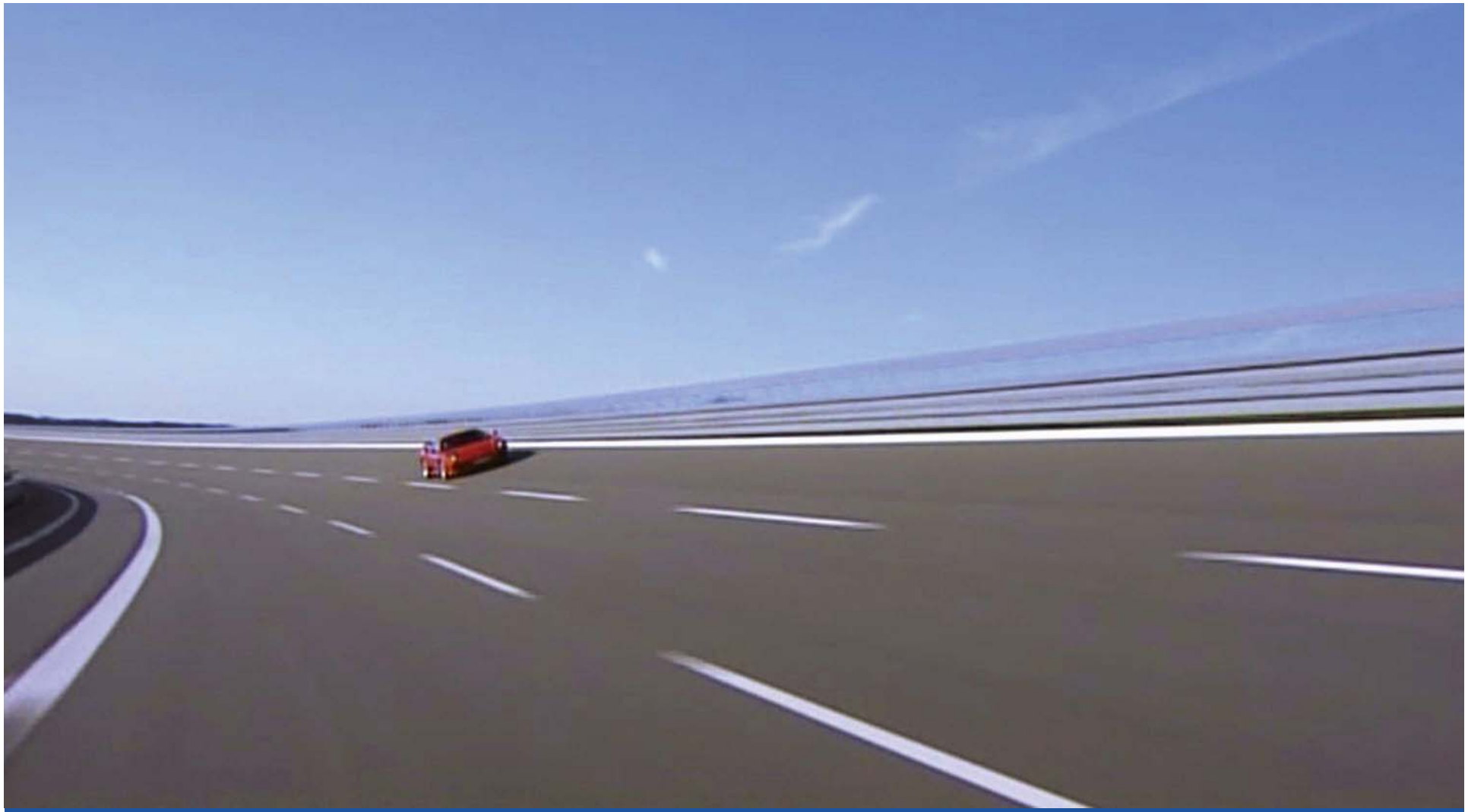
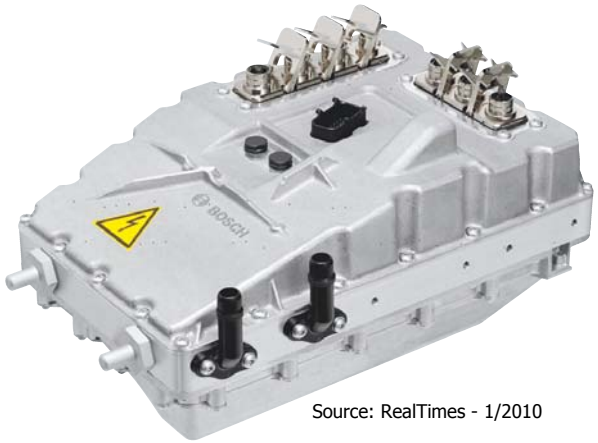
High Dynamic E-Motor-HiL-Testing: PC-based vs. FPGA

Open Technology Forum, 2010 Testing Expo Stuttgart, Germany, 22-06-2010



Challenges with HiL-testing of E-motor control in the lab

- Electric propulsion of passenger cars requires control of power electronics in the range of **50 to >100 kW**
  - Typically, integrated housing of control unit and inverter (high electric power interfaces)
  - Hence, HiL-testing needs handling of electric power, that is significantly higher than in traditional ECU-HiL-applications (power-level HiL)



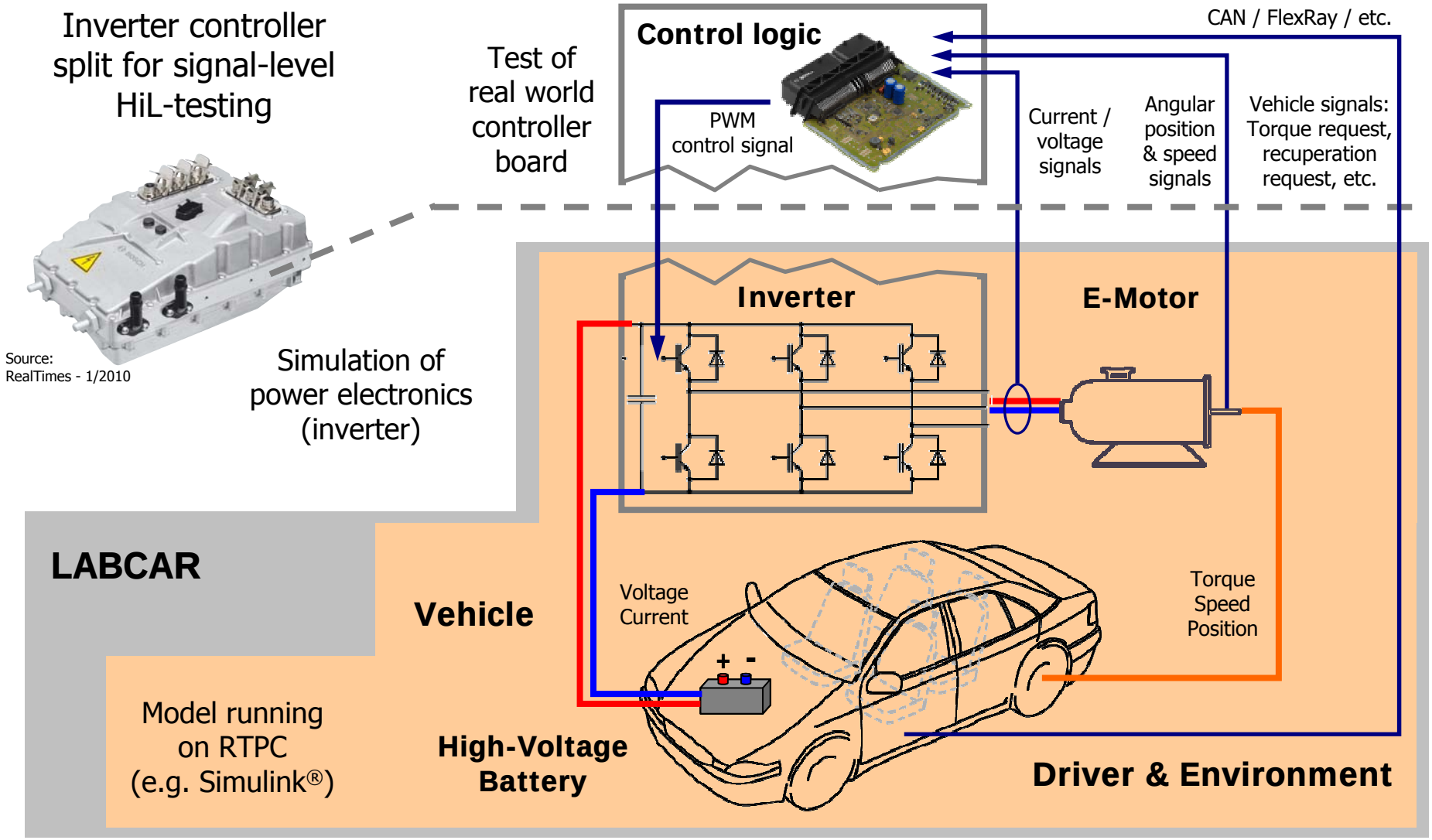
Source: RealTimes - 1/2010

- Highly dynamic electro-magnetic inverter-/E-motor system for electric propulsion of passenger cars requires to compute update-frequency for **control signals in the range of 10-25 kHz**
  - This is significantly higher update frequency compared to traditional ECU-HiL-applications in power-train or chassis control domain

High dynamic E-motor HiL-testing
Agenda

- Benefits of PC-based signal-level-HiL
- The need for low latency plant simulation
- Main advantages of FPGA-based model execution
- Switching between PC-based and FPGA

High dynamic E-motor HiL-testing
Configuration of a PC-based signal-level HiL



High dynamic E-motor HiL-testing
PC-based signal-level HiL

Configuration

- Extract the control logic from integrated control/inverter housing
- Interface on the level of inverter control signals and sensor signals
- Replace E-motor and inverter power electronics by a model

Benefits of signal-level HiL

++ Significantly lower cost for the test system compared to power-level HiL
(no need for high-voltage cabinet and management of high electric power)

Benefits of PC-based model execution

++ Flexible PC-based execution of plant model (e.g. standard Simulink®-based)

\+ No need for special (costly) VHDL-implementation of the model

\+ Almost unlimited compute power for high model granularity

Limitation

— Test of power electronics hardware not covered

— Risk of raster delay under certain conditions
(e.g. left-aligned control signal close to 100% DC)

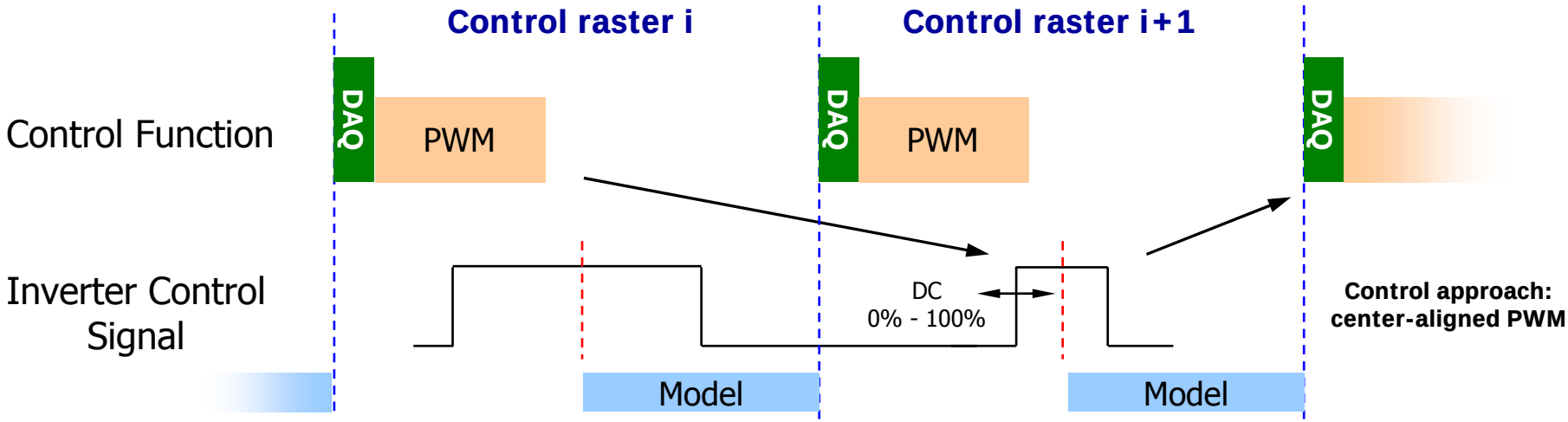
High dynamic E-motor HiL-testing
Agenda

- Benefits of PC-based signal-level-HiL
- **The need for low latency plant simulation**
- Main advantages of FPGA-based model execution
- Switching between PC-based and FPGA

High dynamic E-motor HiL-testing
The need for low latency plant simulation

- Highly dynamic electro-magnetic system requires high accuracy of signal-timing
- Ensure within one control raster (typical 100 µs for 10 kHz control systems):
  - Acquisition and interpretation of inverter control signal
  - Simulation of E-motor reaction and relevant sensor signals

↳ Available time for model computation for center-aligned PWM: max. 25 – 50 µs
(depending on system-specific control frequency; for left-aligned PWM almost zero in worst case)



DAQ — Signal acquisition by control logic

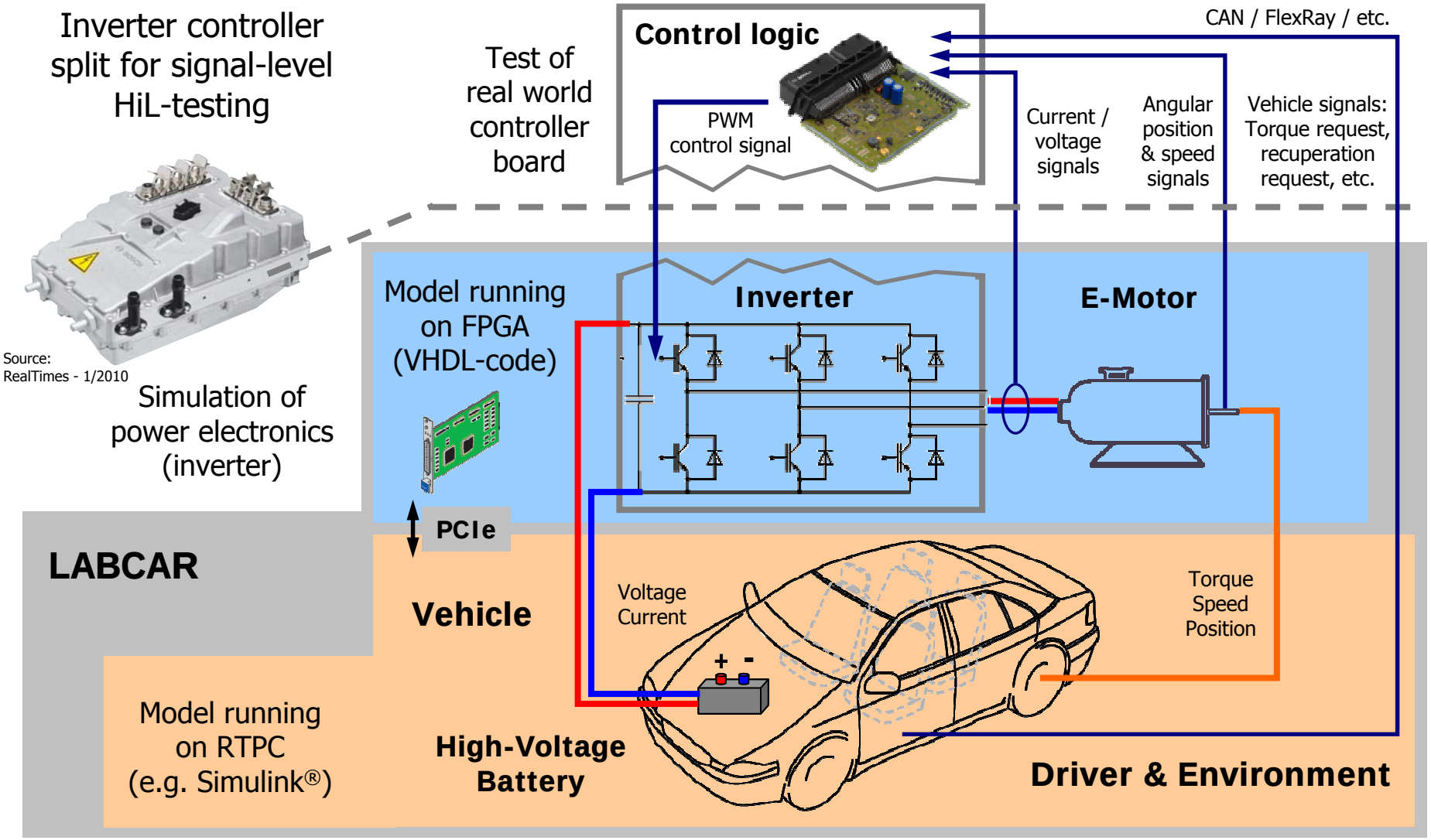
PWM — Compute control signal for next raster

Model — Time for model computation on HiL

High dynamic E-motor HiL-testing
Agenda

- Benefits of PC-based signal-level-HiL
- The need for low latency plant simulation
- **Main advantages of FPGA-based model execution**
- Switching between PC-based and FPGA

High dynamic E-motor HiL-testing
Signal-level HiL with model execution on FPGA



High dynamic E-motor HiL-testing
Model execution on FPGA

Configuration

- Same hardware set-up as with RTPC-based signal-level HiL
- Inverter and E-motor model is implemented in VHDL-code for FPGA
- Model execution on-board the multi-I/O-board ES5340
- PCIe-interface with vehicle/driver/environment modules running on RTPC

Main benefits of FPGA-based model execution

++ Quasi-continuous plant simulation (model execution time ≤ 1 µs)
  - ↳ Simulation of inverter and E-motor directly following the control signal
  - ↳ No risk of raster delay (in typical HiL-applications)

\+ Simulation of switching-ripples inherent

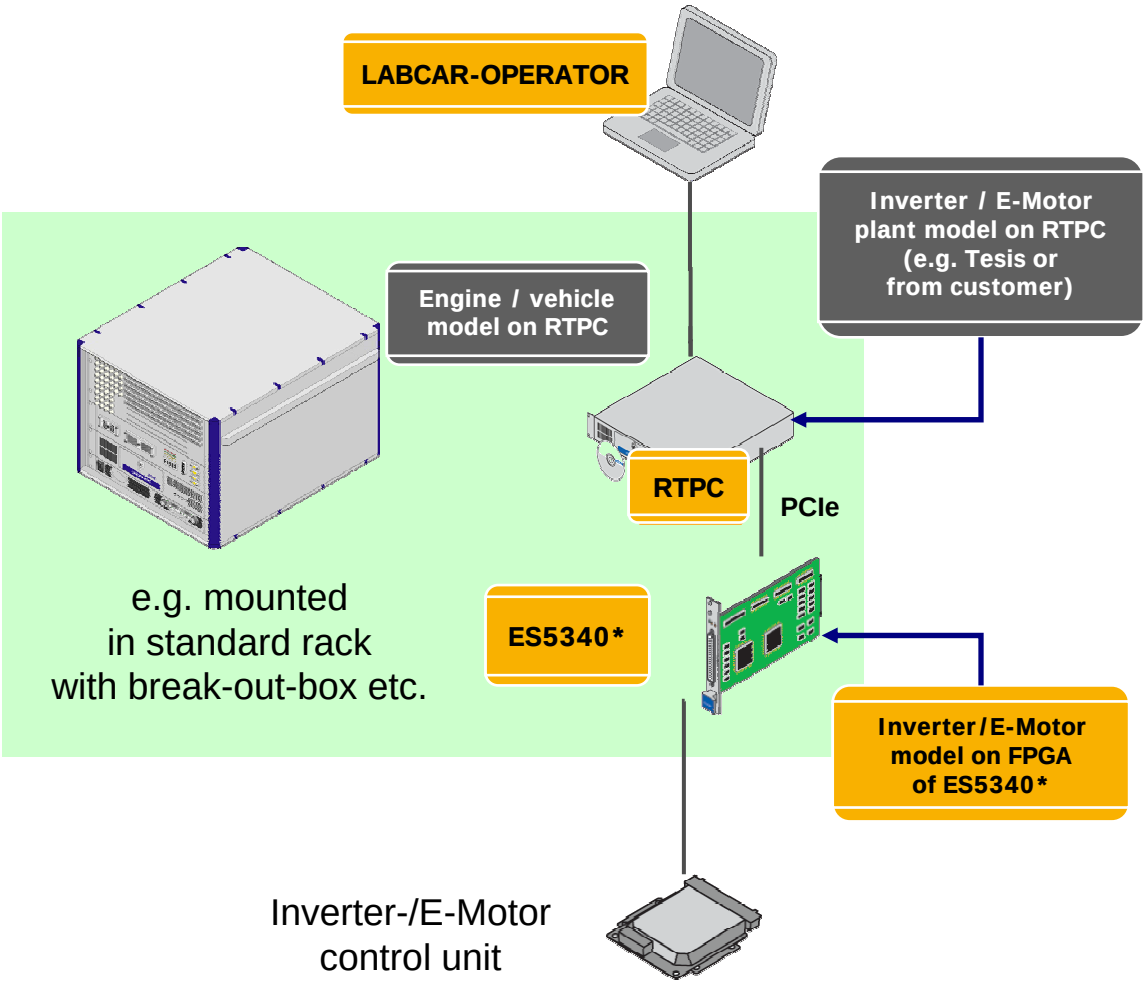
Limitation / remark

○ Implementation of reliable and efficient VHDL-code for FPGA needs special expertise (even when applying FPGA-development framework for Simulink®)

High dynamic E-motor HiL-testing
Agenda

- Benefits of PC-based signal-level-HiL
- The need for low latency plant simulation
- Main advantages of FPGA-based model execution
- Switching between PC-based and FPGA

High dynamic E-motor HiL-testing
RTPC- or FPGA-based LABCAR without changing hardware



- FPGA-model can be installed on ES5340 by standard firmware update kit
- No change of hardware components needed
- Parameterization of FPGA-based model via LABCAR-OPERATOR
- Real-time interface with vehicle/driver/environment models running on RTPC available in both variants

* Product release planned Q4/2010

High dynamic E-motor HiL-testing
Summary

- New PCIe-board ES5340 provides ready-to-use multi-I/O functionality for signal-level HiL-testing of Inverter-/E-Motor control
  - Product release E 2010
  - Intermediate solutions already available (ask for migration-option towards ES5340)
- FPGA of ES5340 enables on-board model execution
- Hence, both variants available for Inverter-/E-motor model:
  - RTPC-based model execution (pin-to-pin latency ≈ 20 µs)
    - ↳ Highly flexible
    - ↳ Cost-optimized
  - FPGA-based model execution (pin-to-pin latency ≈ 1 µs)
    - ↳ Quasi-continuous plant simulation → no risk of raster delay
    - ↳ Simulation of ripples introduced by inverter switching
- RTPC- or FPGA-based model execution possible without adding or changing any hardware component

Thank you

谢谢

धन्यवाद

Merci

有難うございました

감사합니다.

Muchas gracias

Vielen Dank