Auto generated Remaining Bus Simulations based on a Fibex description file

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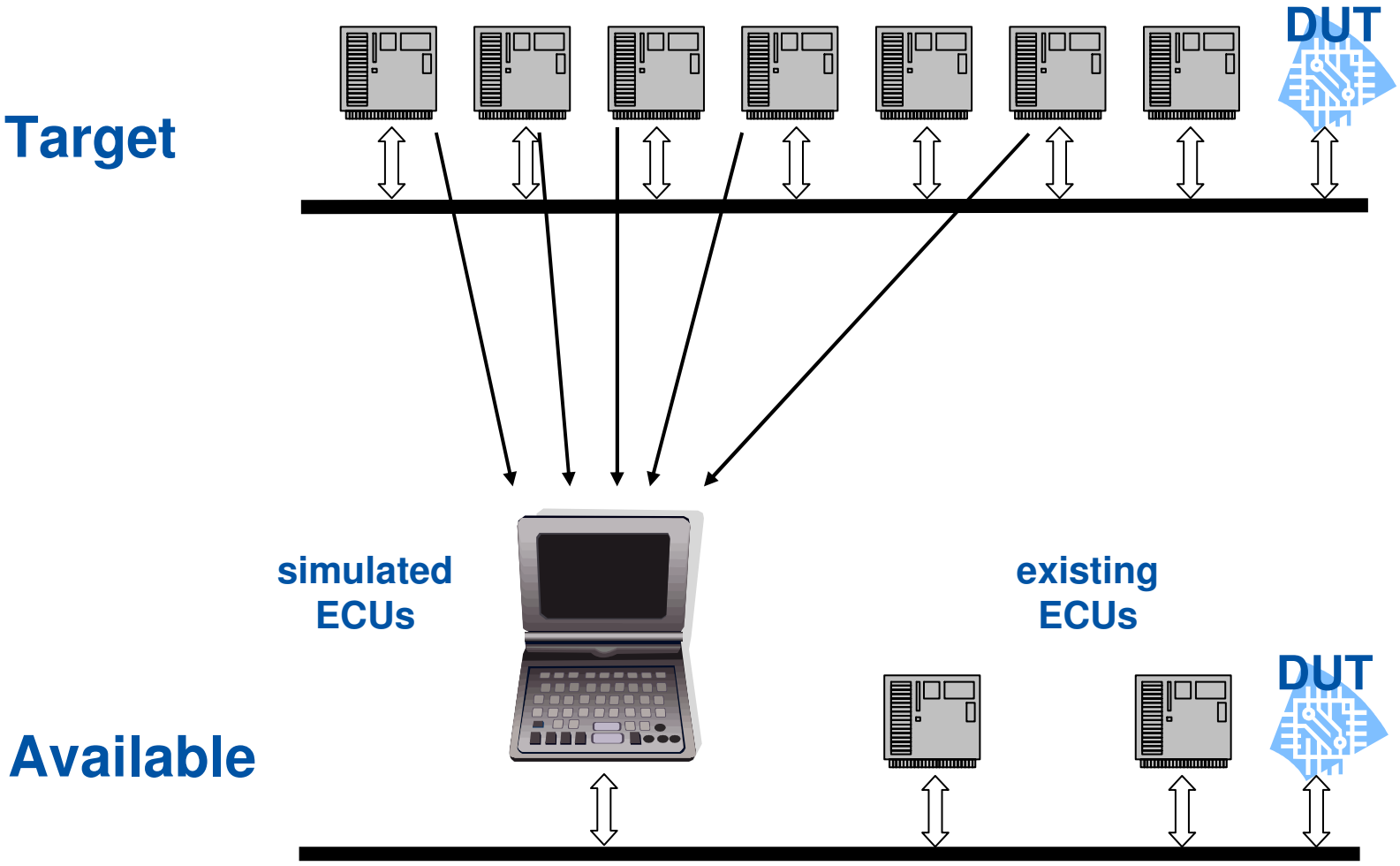
A company of Steinbeis GmbH & Co. KG für Technologietransfer

Contents

- What is a RBS?
- RBS - Why?
- Needed features
- Fibex as database
- Concept
- Implementation
- RBS vs. HIL
- Example

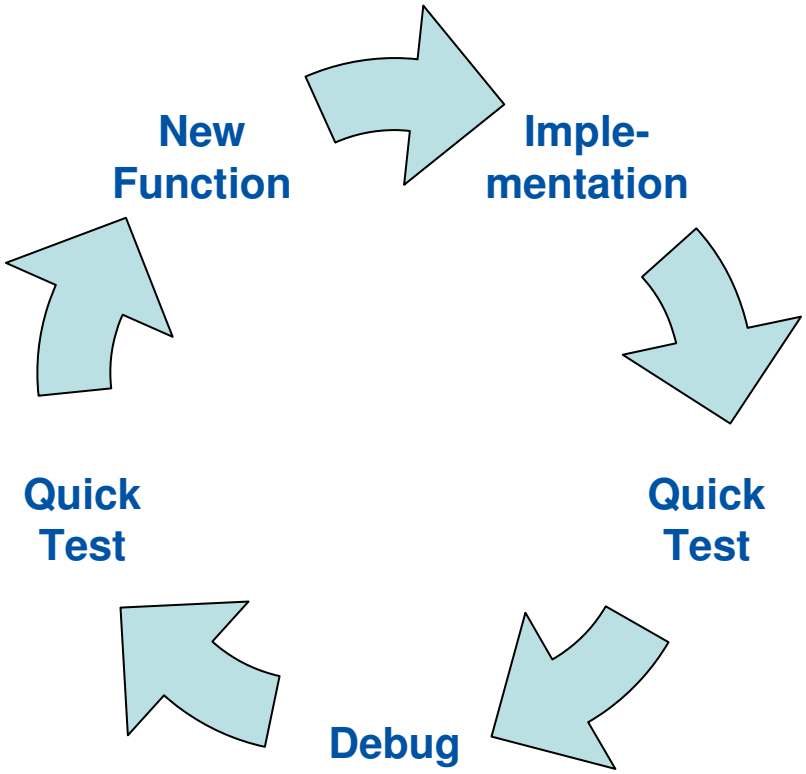
What is a RBS?



RBS – Why?

- **Testing**

  During Development: Verify new implemented functions

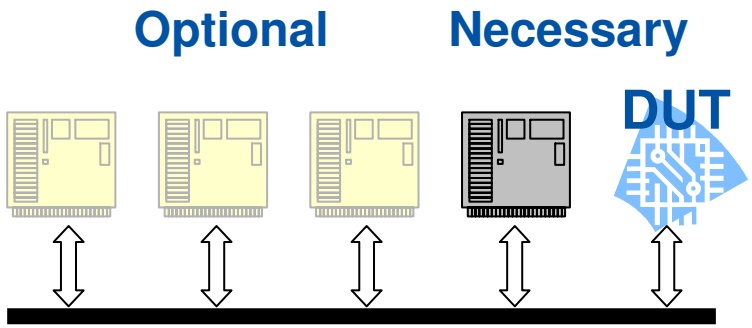


RBS – Why?

- **Keep Bus Alive**

  Two Nodes necessary

  - Startup
  - Synchronization



- **Device under test needs correct bus data**

  Dataflow control in real-time

  - Alive counter
  - CRC

RBS – Why?

- **Behavior verification**
  - Startup
  - Shutdown
- **Verification of FlexRay Parameter**

  Configuration quite complex
  - DUT synchronizes
  - DUT sends Frames
  - DUT does not cause errors

Needed Features

- **Fast generation of the RBS (5-10 min)**

  Complete auto generation of the RBS out of a description file (FIBEX)

- **Application CRC calculation**

  Application CRCs must be included on certain positions.
  CRC algorithm defined by the user.

- **Alive counter calculation**

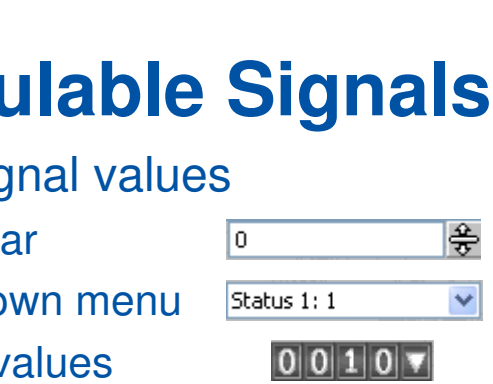
  Alive counter must be included on certain positions.
  Algorithm defined by the user.

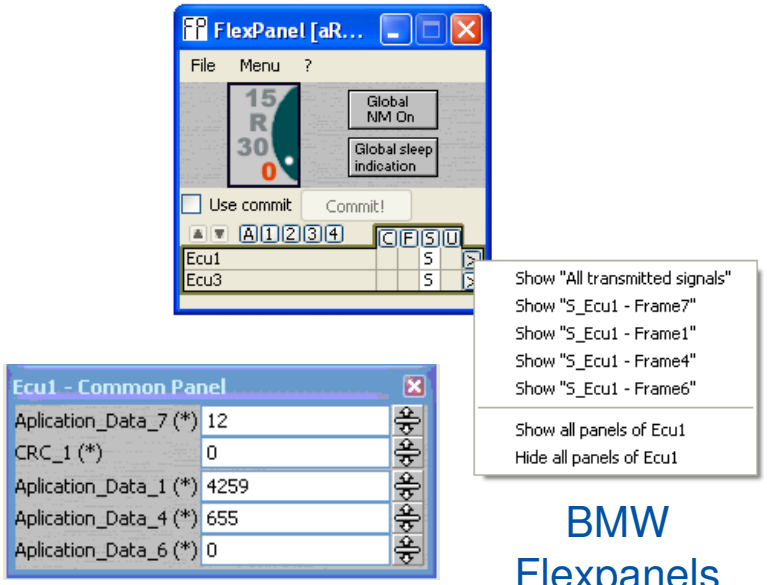
Needed Features

- **Manipulable Signals**

  Change signal values

  - Scroll bar
  - Drop down menu
  - Binary values





BMW Flexpanels

- **Adaptation to the integration process**

  Exclude already existing frames / ECUs

Needed Features

- **Monitor bus traffic**

  In error cases it is helpful to be able to have a look at the bus traffic.

- **Includable User defined code**

  An user interface should be provided to define user code which shall be included during code generation.

- **Deadline-/Overload-Monitoring**

  Insurance that the simulation works correct

  - Deadline violations
  - Losing Frames
  - CPU too weak (User code)

Needed Features

- **NM support**

  Network management functionality must be supported.

- **Control / error indication / special functions**

  Diagnose functions beside normal operation mode

  - Alive Counter manipulation
  - Application CRC manipulation
  - Header CRC manipulation
  - Calculation stop
  - Defined and repeatable synchronization and shut down

Advantages of FIBEX

- **Standard format in the automotive section**

  Nearly every firm uses FIBEX to describe there busses.

  FIBEX is supported by many tools.

- **Nearly everything is describable**
  - Bus parameters
  - Bus topology
  - ECUs
  - Signals
  - Frames

Disadvantages of FIBEX

- **NM not supported**
  - Payload-Preamble-Bit not supported.
  - Autosar NM planed in Fibex 3.0.1

- **Fast update rate**

  Short intervals between new FIBEX version

  ➔ A lot of work to keep the tools / database up to date.

Roots

The following remain bus simulation is based on a concept of

BMW AG
Forschungs- und Innovationszentrum
80788 München
Dr.-Ing. Robert von Häfen
Dipl.-Ing. Georg Fries (Reliatec GmbH)

A patent is pending

AZ: 102007002312.1

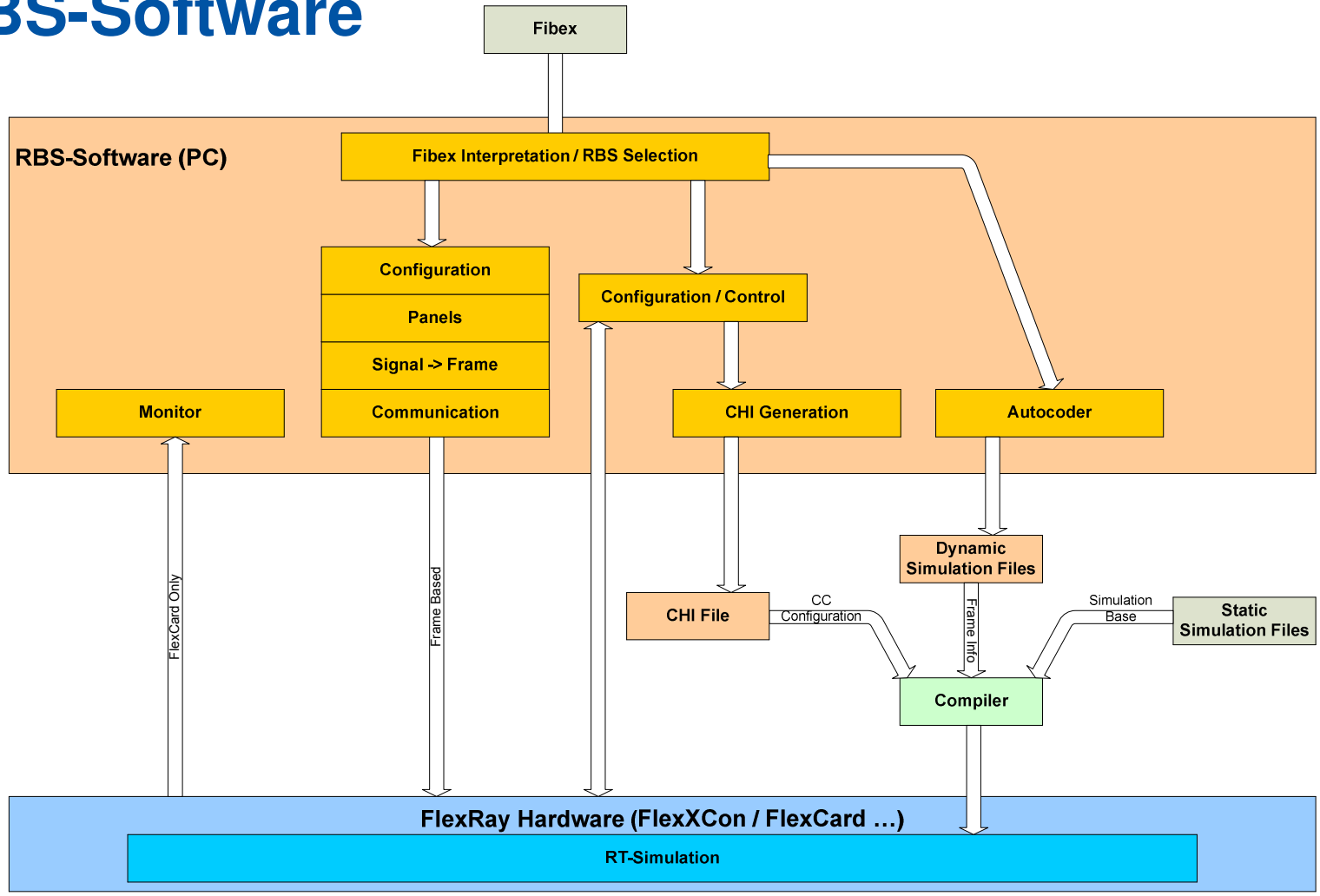
Concept

Principle:

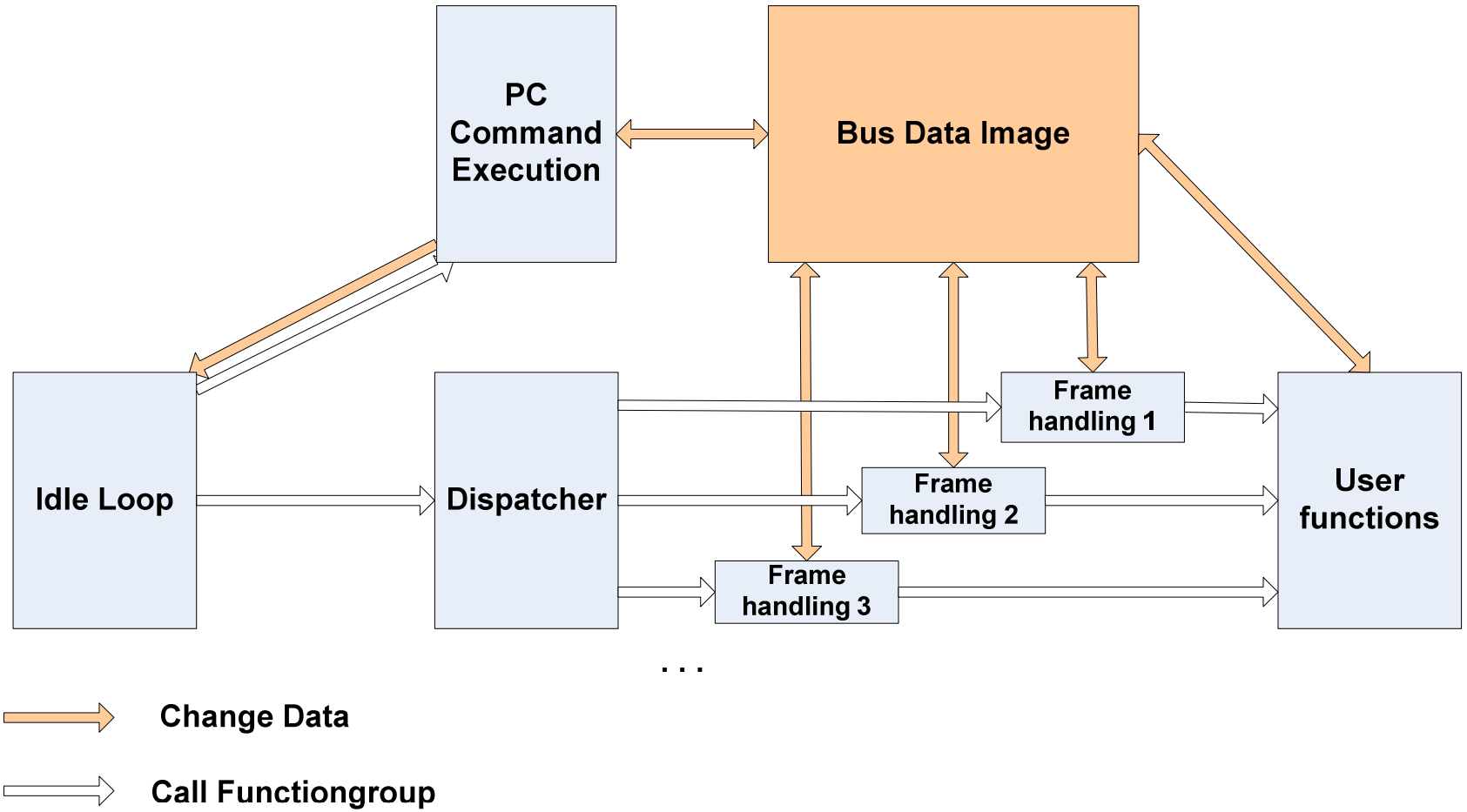
- **Separating the software in a real-time and a non-real-time part**
- **Use a real-time platform and PC for corresponding software parts**
- **Make an intelligent simulation of the remaining bus communication**

Concept

RBS-Software



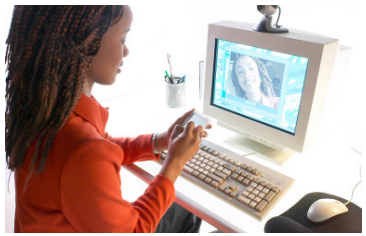
RBS-Firmware



RBS vs HIL

RBS:

Human controlled



PC connection (PCI / Ethernet …)

FR bus

DUT

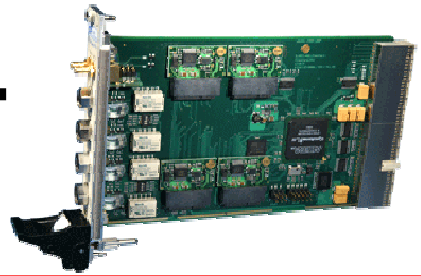
Non-real-time | Real-time

HIL:

IO
Sensor
Actor

Model controlled

PC connection (PCI, …)



FR bus

DUT

Real-time

RBS vs HIL

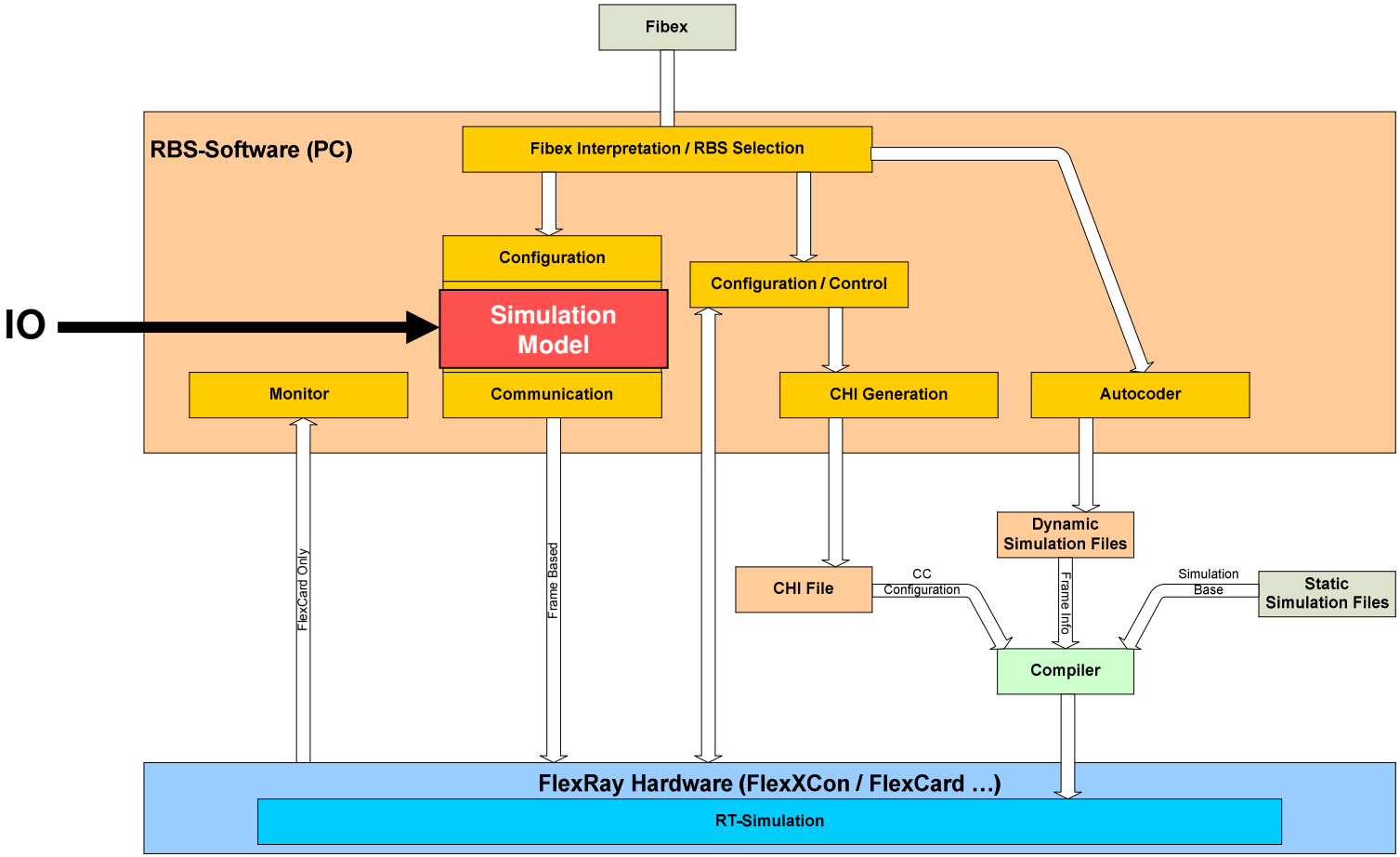
RBS

- Elementary / Cheap
- Real-time at lower level
- Short generation time
- Human controlled test
- Step by Step Testing
- Less error-prone since auto generated

HIL

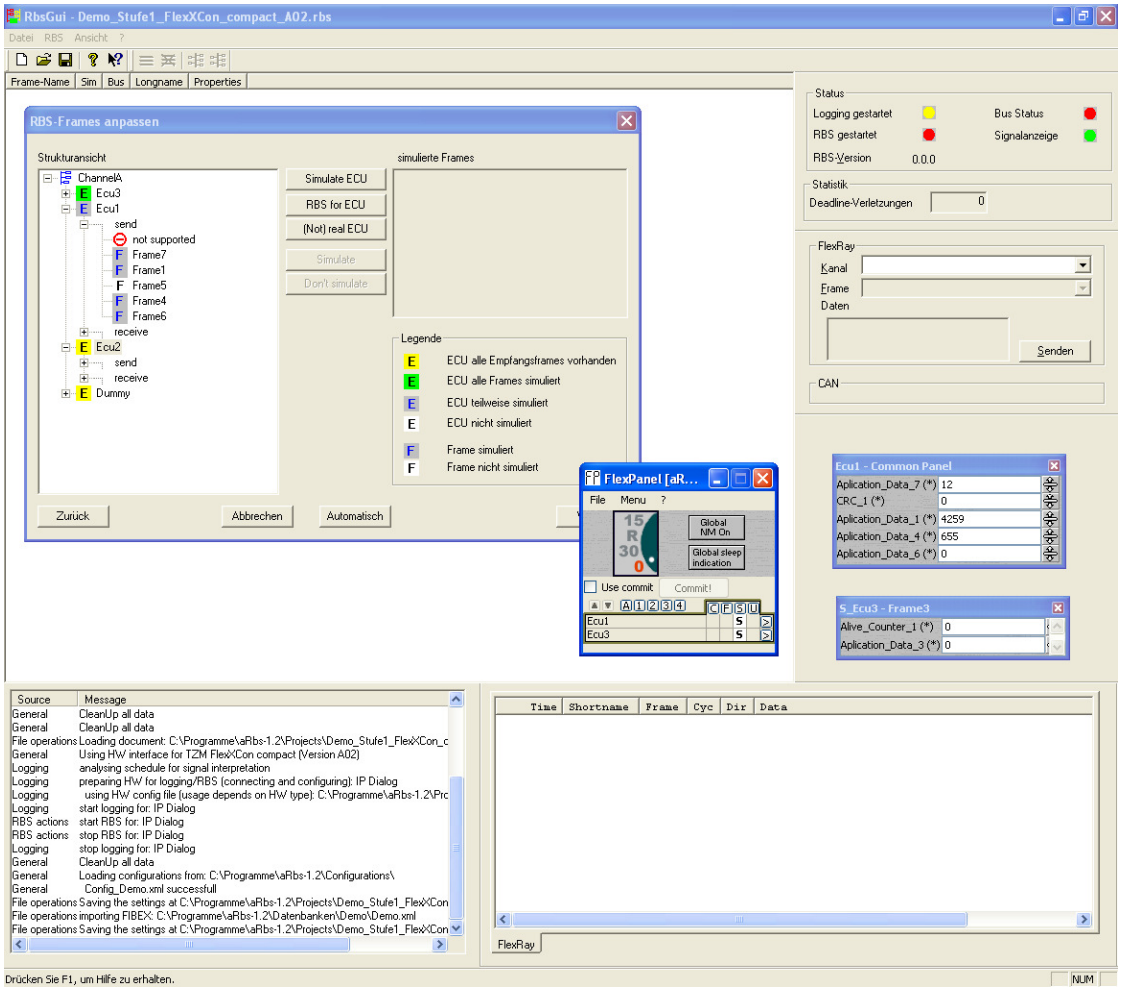
- Complex / Expensive
- Real-time at every level
- Time intensive model generation
- Automated test (model, parameter controlled)
- Test normally not interruptible
- If an error appears, is the error in the DUT or in the simulation model?

Transform the RBS into a HIL



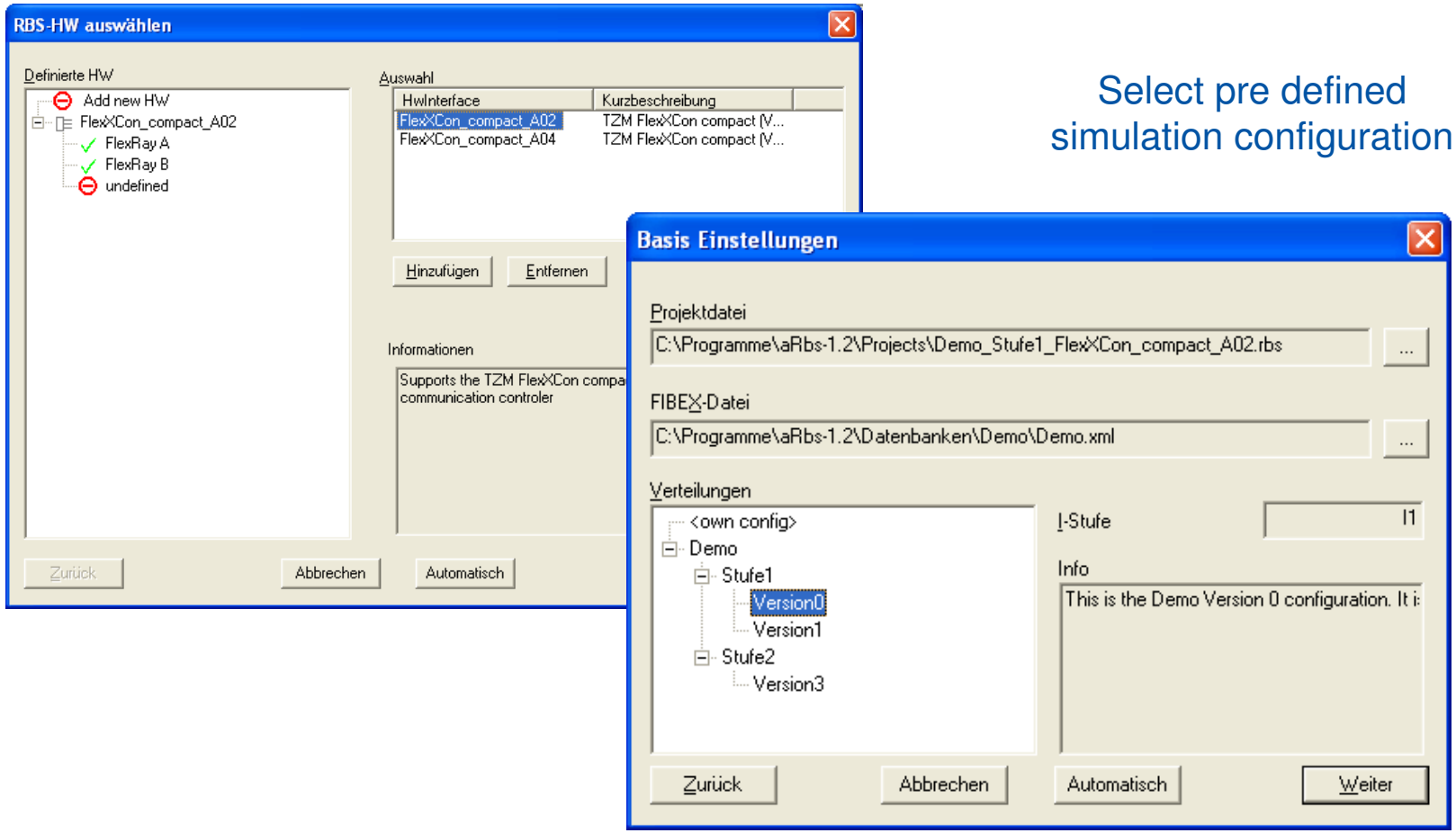
Example

FlexRBS



BMW GUI

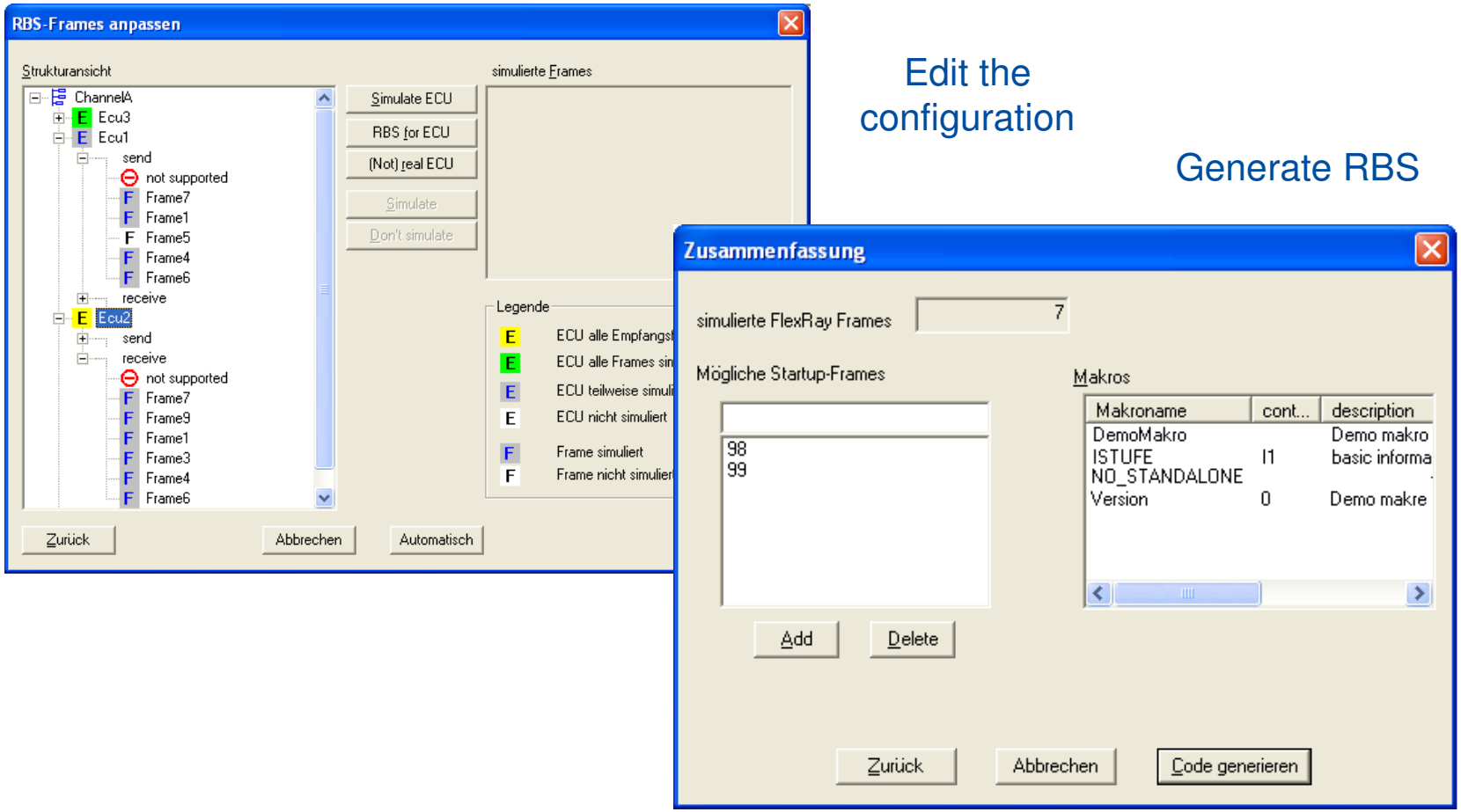
FlexRBS - Workflow



Select pre defined simulation configuration

Example

FlexRBS - Workflow



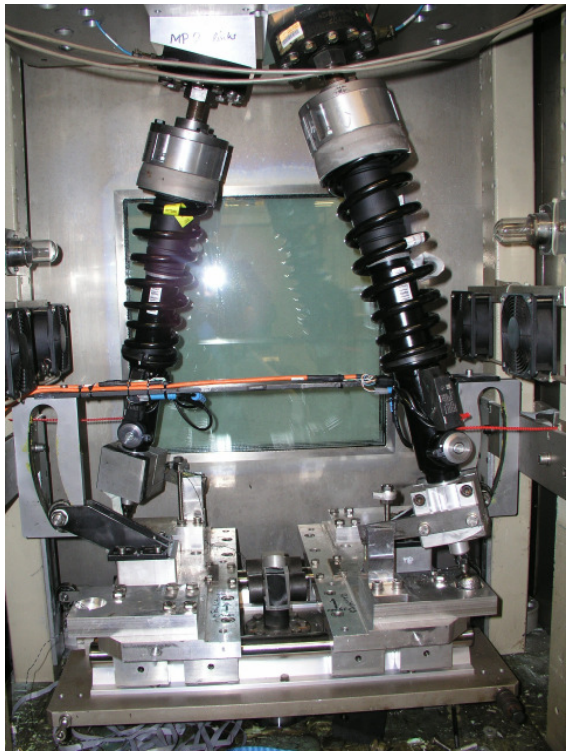
Edit the configuration

Generate RBS

Example

Restbussimulation at BMW

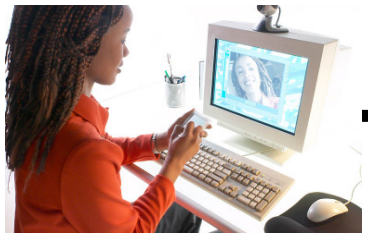
Test bench for dumpers



Example

Restbussimulation used for pre-verification

Reference Traffic

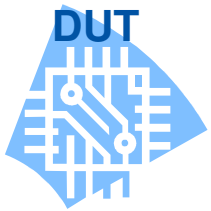


FR bus

=

Produced Traffic

FR bus



Conclusion

- Can not replace a HIL system, but is a cheap test alternative to minimize the test time at the HIL system
- Quick creation
- Useful test tool during development

Thank you for your attention

Questions?

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