

A Transparent Solution for Providing Remote Wired or Wireless Communication to Board and System Level Boundary-Scan Architectures

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The logo for Patria, featuring the word "Patria" in a bold, blue, sans-serif font on a white background.The logo for JTAG Technologies, featuring the letters "JTAG" in a large, blue, serif font, with the word "Technologies" in a smaller, blue, sans-serif font below it, all on a white background.

Purpose

- It's becoming increasingly difficult to gain access to board level boundary-scan test infrastructures using the traditional 5-pin IEEE 1149.1 interface.
- This presentation describes a transparent solution for providing remote access to single or multi-board boundary-scan architectures using the products existing wired or wireless communication protocol.

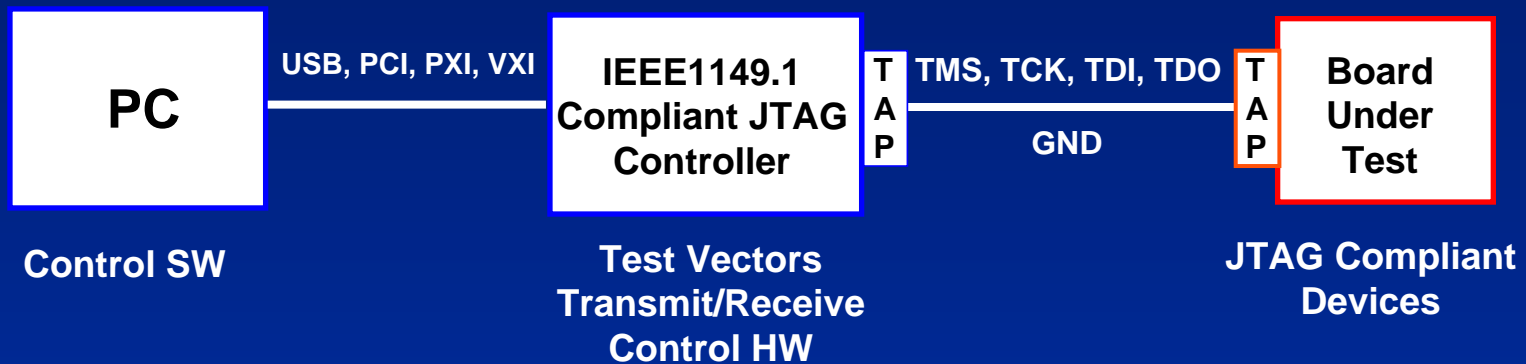
Outline

- Introduction
 - Overview of boundary-scan test strategies.
 - Problems in using the traditional 5-wire interface.
 - Remote test access considerations.
- The Solution
 - Stand-alone and embedded solutions.
 - Testing within network environments.
 - Operational benefits and principles.
 - Hardware and software requirements.
 - Performance considerations.
- Conclusions

Overview of Boundary-Scan Test Strategies

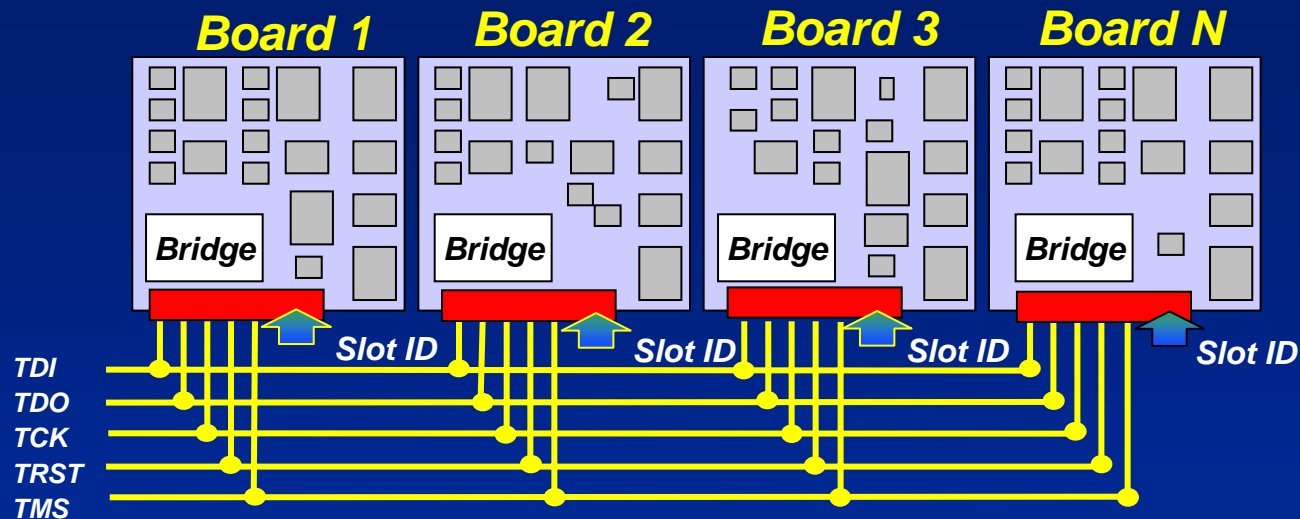
- Boundary-scan is used extensively throughout the electronics industry for providing high test coverage.
- Emphasis on using the device Test Access Port (TAP) to gain access to 1149.1 test infrastructure and embedded BIST test structures.
- The availability of system level multidrop address, test access devices has extended boundary-scan testability to the system environment.
- Providing access to device, board and system level 1149.1 test infrastructures is a prime DFT objective.

Problems in Using the Traditional 5-wire Interface



- Connection between boundary-scan test controller and target design is through a wired connection.
- It is conceivable that design to be tested has no physical space for 5 dedicated boundary-scan pins. This is emphasized for fully assembled products.

Problems in Using the Traditional 5-wire Interface

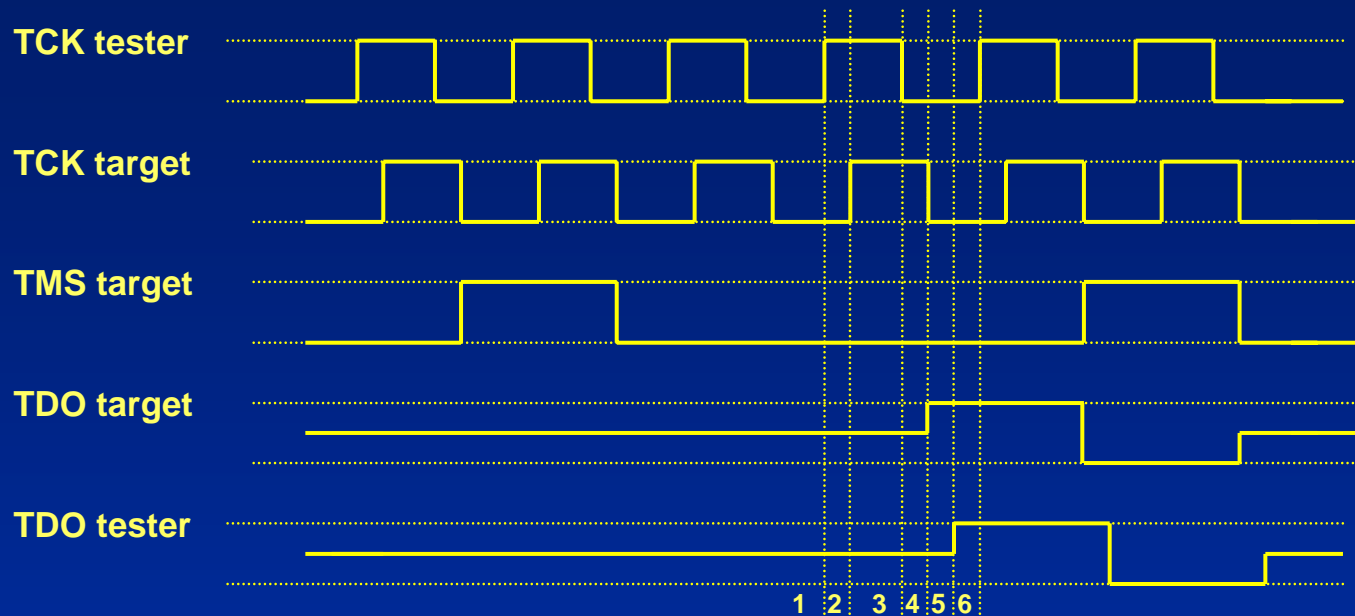


- 1149.1 hierarchical multidrop architectures require a dedicated 5-wire boundary-scan bus and access to the board level infrastructure via the edge connector.
- This is not always possible due to physical access limitations or the remote location of the application i.e. satellite systems.

Considerations for Remote Testing

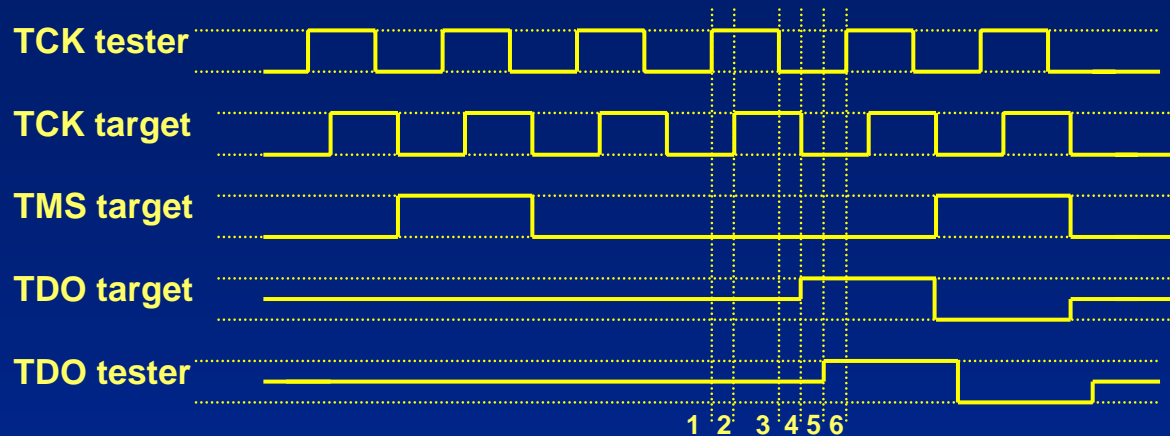
- It's desirable to utilize the target system's existing communication channel.
- This requires some mechanism for transporting boundary-scan information, using either a wired or wireless interface.
- There are 3 issues that need to be addressed
 - Physical access to the board-under-test (BUT)
 - Transmission delays in accessing the BUT over a large distance
 - Cost factors, e.g. design complexity

Transmission Delay Considerations



- On the rising edge of TCK (2) target devices sample TMS and TDI.
- On the falling edge, TDO data (4) is updated and sent back to the test controller (5).
- The test controller expects TDO data on the rising edge of TCK (6).

Transmission Delay Considerations



- The amount of time for TDO data to travel from the last boundary-scan device (4) to the test controller (6) is half the TCK period.
- If TCK frequency is 10 MHz (clock period of 100 ns) this only allows total of 50 ns for cable & transceivers.
- If propagation delay of cable is 5 ns/m, a maximum cable length of less than 10 metres is only possible.

Remote Test Access Possibilities

- Reliable, yet simple hardware solution for remote maintenance, configurations and updates.
- Transparent access to virtually all remotely located targets, such as distributed automation systems.
- Flexible access enables advanced tests without the cost of embedding them in (vectors storage).
- A remote 'prognostics' and 'diagnostics' capability may be considered more valuable than raw TCK rate.

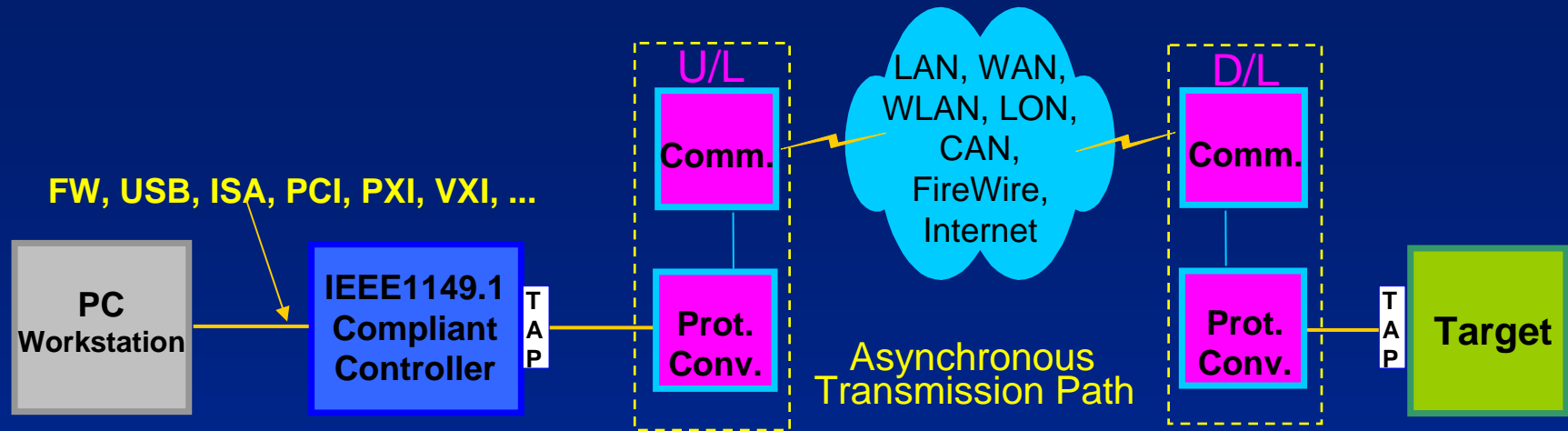
Remote Test Access Concerns

- 1149.1 Standard does not support data encryption or decryption.
- 1149.1 System level access devices do not provide error detection and error correction (addressed by the discontinued 1149.5 MTM bus standard).
- 1149.1 Deficiencies can be handled by a higher level protocol.

Remote Test Access Security

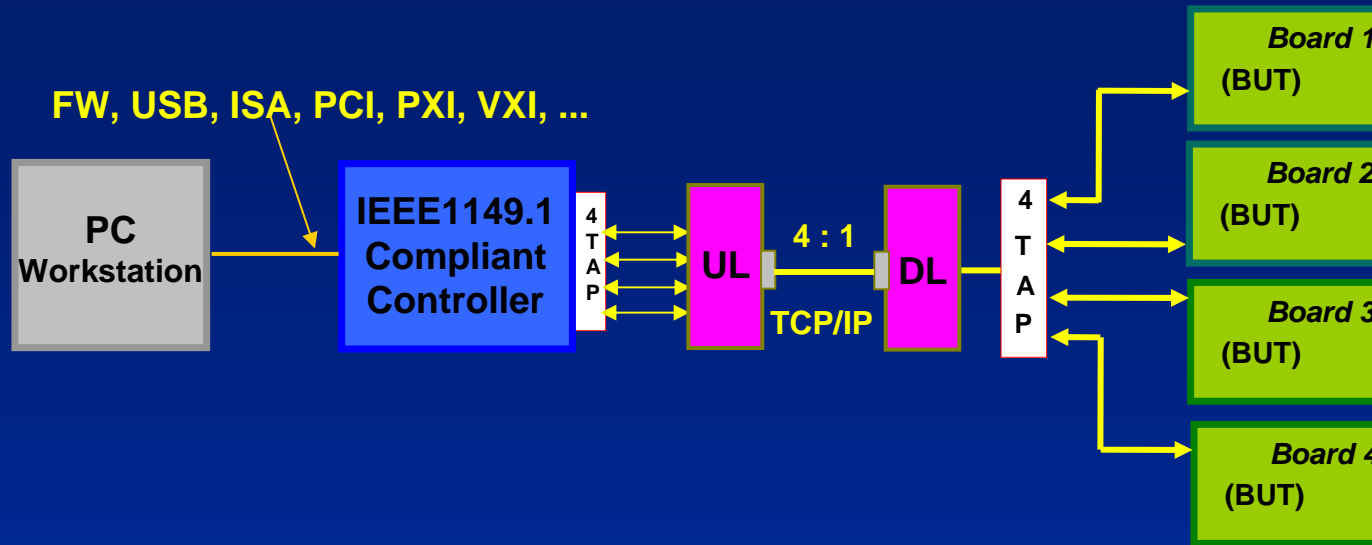
- Sensitive IEEE-1149.1 data can be embedded inside a high-level tamper proof, error tolerant protocol.
- No difference to normal data protection schemes within existing communication protocols, such as TCP/IP support error detection and correction.
- Existing communication medias and protocols, such as GSM and WLAN WEP, may also provide strong data encryption and authentication.

The Solution



- At the boundary-scan controller, the TAP signals are coded to the communication protocol and then transmitted via the communication link to the target.
- At the controller an UpLink Module (U/L) is present for the protocol conversion and communication.
- At the target a DownLink Module (D/L) is present for the protocol conversion and communication.

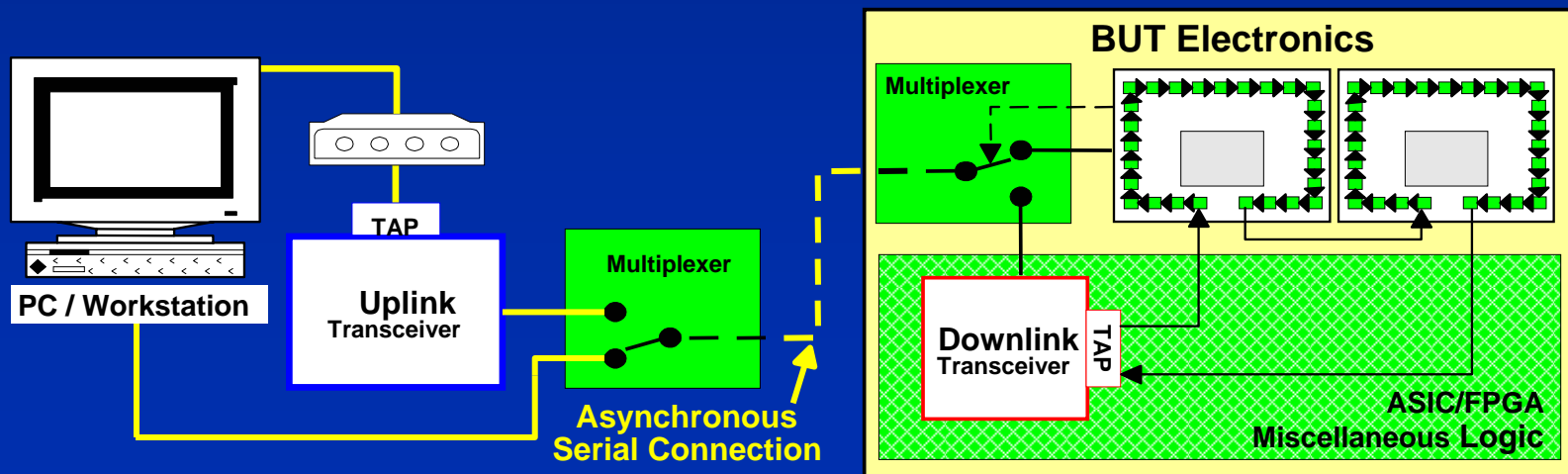
Parallel Testing



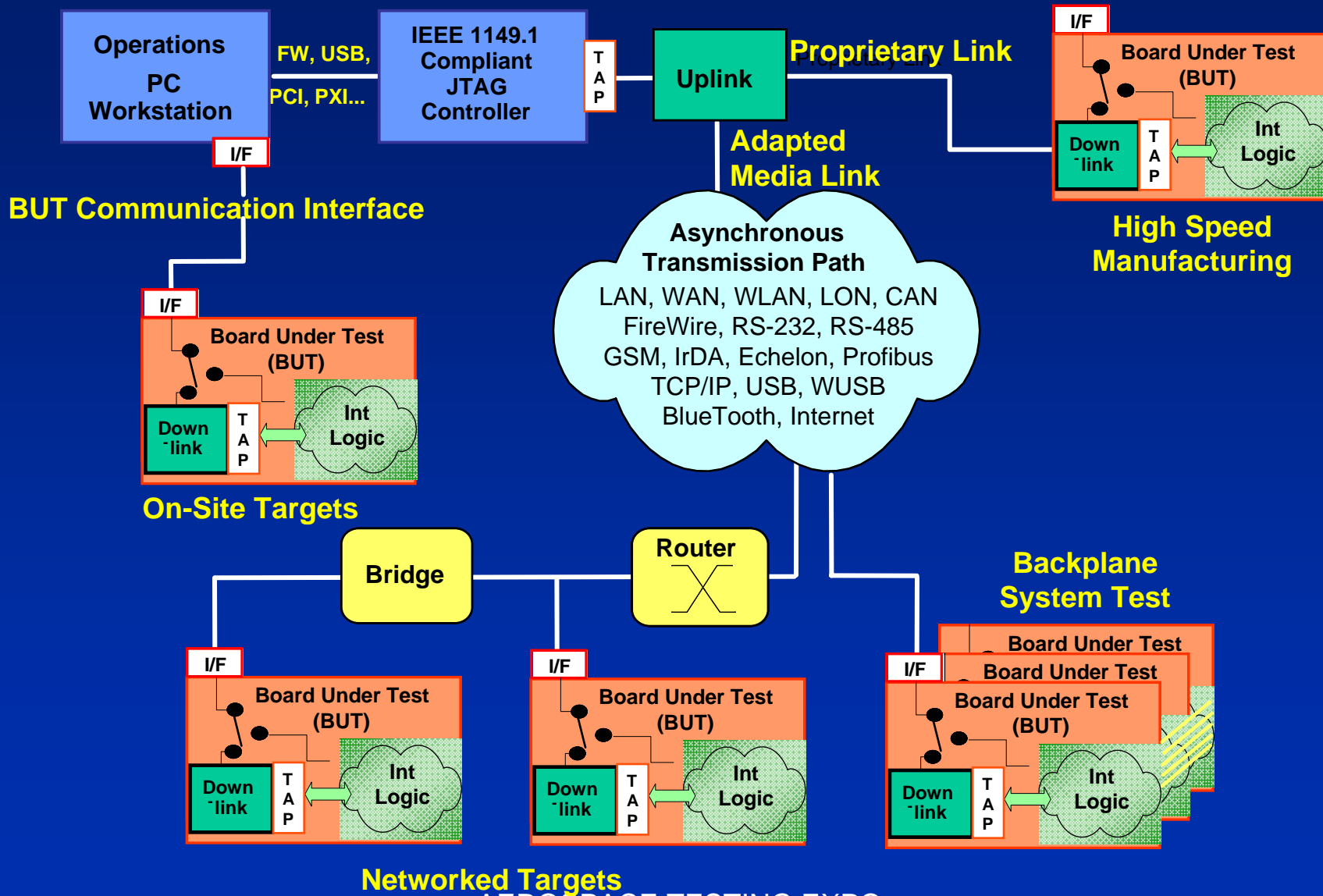
- Supports the concept of parallel testing by allowing access to multiple chains/boards within a single system i.e. 'gang' testing.
- The 4:1 serialization may introduce performance degradation due to bandwidth limitations, but this is compensated by the ability to test multiple boards simultaneously.

Embedded Solution

- BUT may be used normally via communications link, and optionally switched to testing mode.
- Downlink is embedded into the BUT (< 1k gates).
- BUT's communication link is multiplexed with the Uplink and Downlink transceivers.
 - Multiplexing is controlled by communications protocol



Networked Solutions



Networked Targets

AEROSPACE TESTING EXPO
2005

Testing in a Networked Environment

- Can be used in any network environment with suitable Uplink interface adapter.
- Downlink can be stand-alone which is attached to network with a standard TAP-connection to the BUT.
- Downlink can be embedded into the BUT and the test access is gained via existing com-link.
- System level tests can be integrated from modular tests and transported via existing com-link.

Testing in a Networked Environment (access to multiple targets)

Can share one Uplink with multiple Downlinks once the communication channel is set-up



Operational Benefits

- **Test data reuse:**

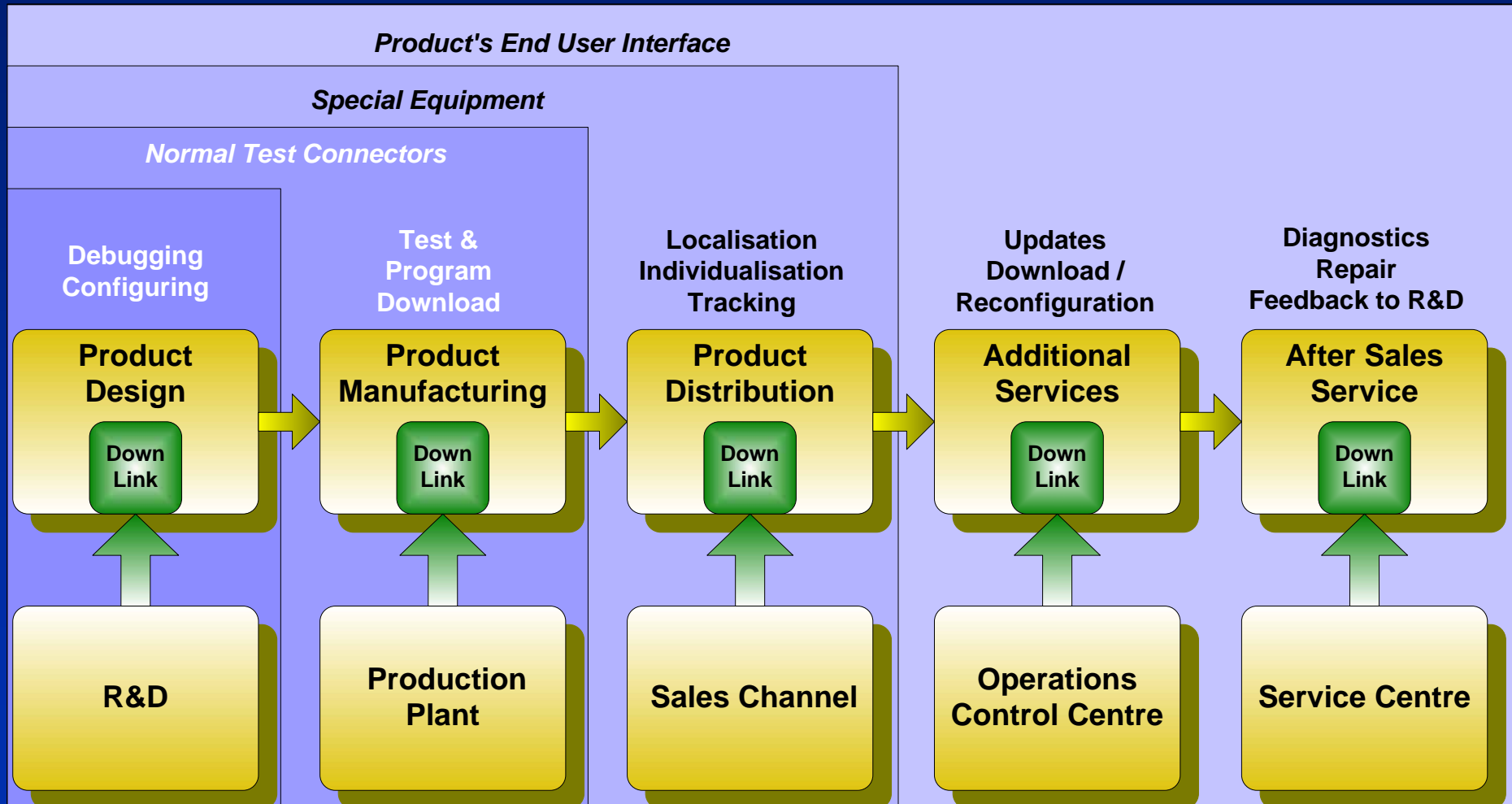
Same tests, configurations and updates can be applied to units from design start to after sales.

- **Test access reuse:**

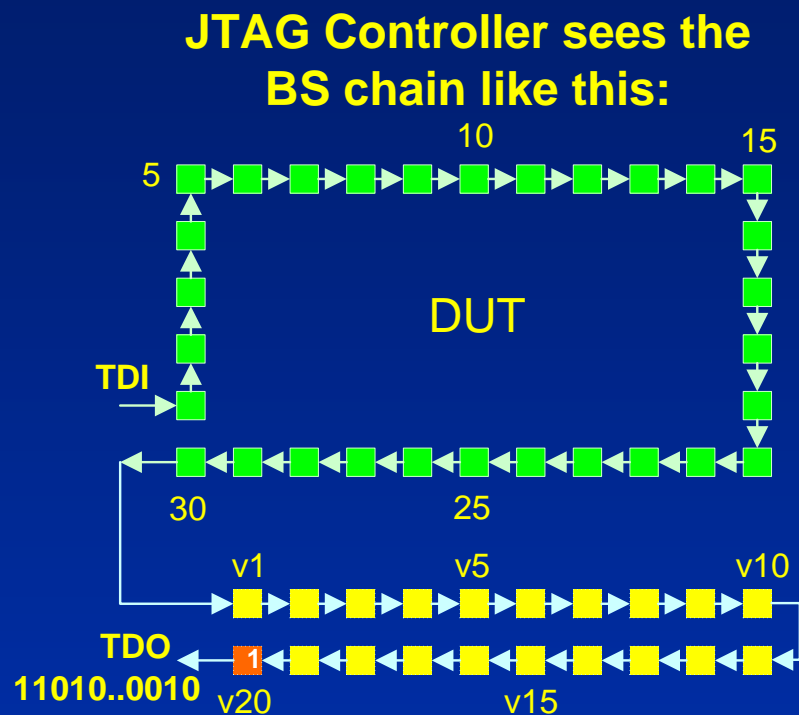
Same communication link can be used from prototype boards to fully assembled products.

Operational Benefits

Same accessibility over the whole Product Lifecycle



Operation Principle

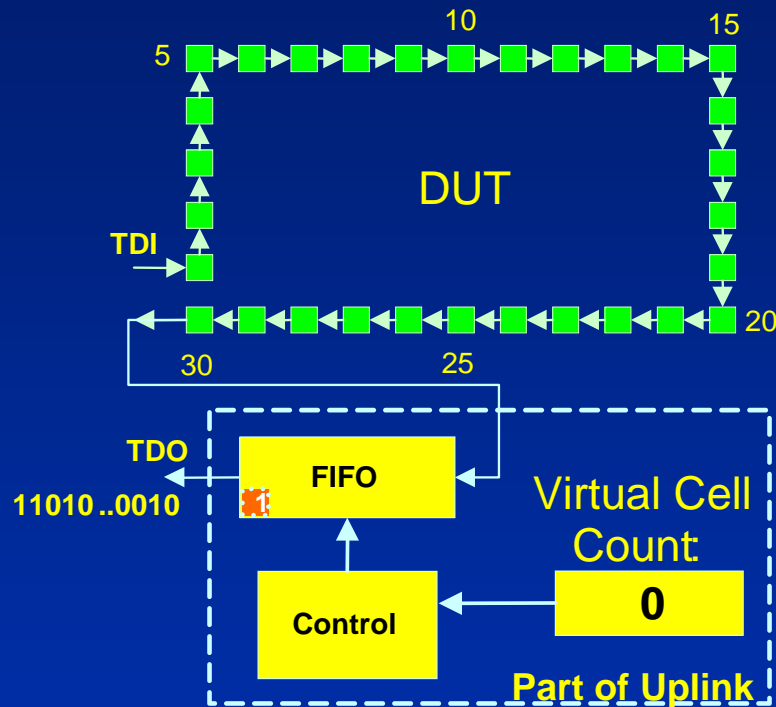


- To allow TCK to run at optimum frequency a virtual component containing virtual cells is appended to the chain.
- The latency of the com link & TCK frequency will dictate the number of cells.

- Additional time is gained for compensating inherent transmission delays during the time when test controller shifts the 'non-existing', virtual cells.

Operation Principle

The real hardware looks like this :



- TDO is incoming to the FIFO buffer asynchronously in respect to TCK
- The Uplink will store TDO data and the 'virtual cell' counter is preset to a pre-determined value.
- The 'virtual cell' counter will decrement every TCK cycle.

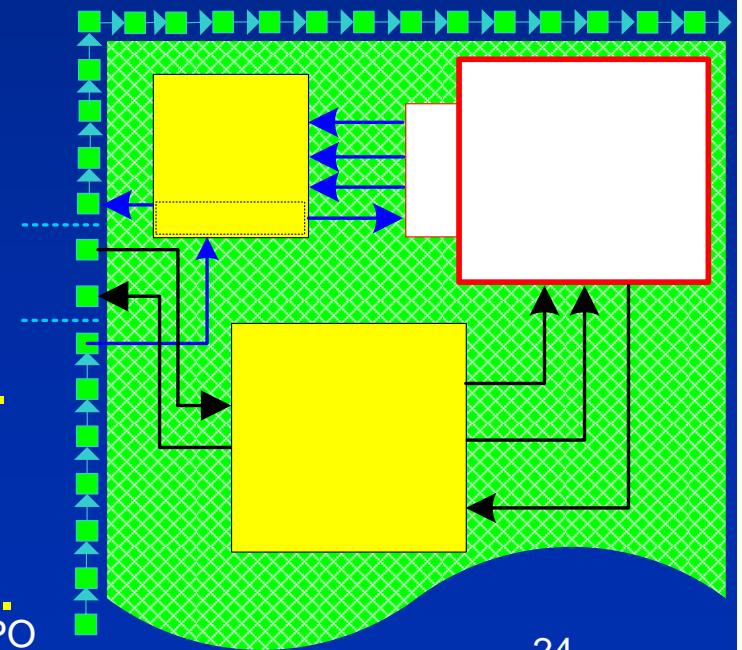
- Once the count value reaches zero, the Uplink will start transferring real TDO data to the test controller for comparison.

Hardware Requirements

- Two bits of information (TMS and TDI) are transmitted in from Uplink to Downlink transceivers per TCK cycle.
- In most cases TMS and TDI data can be transmitted immediately, but depending upon transmission media some small sending buffer may be needed.
- The TCK clock is generated locally by the Downlink upon receiving a valid data packet.
- Only one bit of TDO data (only when valid TDO data is present) is transmitted from the Downlink to Uplink per TCK cycle. Resultant TDO data is temporarily buffered.

Hardware Requirements (Embedded Downlink)

- Embedded Downlink requires minimal logic and is easily built into an existing device i.e. FPGA or ASIC.
- No need for test vector storage memory.
- Test mode selection with communication protocol or with an external signal.
- 1149.1 TMS, TDI reception and TDO transmit may utilize product's existing transceivers, protocol encoders and decoders.
- Removal of the redundant board 1149.1 external test connections.



Software Requirements

- No changes are necessary to COTS boundary-scan test software as the implementation is in hardware.
- A software utility controlling Uplink is required to:
 - Set-up the communication channel between Uplink and Downlink
 - Set-up the operational TCK frequency
 - Perform a loop-back test to determine the channel latency & calculate the optimum number of virtual cells, plus some margin for channel variations
- If communication channel is point-to-point, the inherent latency is pre-determined & virtual cell count known.

Performance Considerations

- A packet based communication protocol is inefficient when compared to the standard 1149.1 pipelined architecture.
- These inefficiencies are compensated by the fact that communication is possible to remote systems using the targets existing communication channel.
- The performance is only limited by the effectiveness of the existing communication channel, not by the time latency introduced by cable length.
- High speed 1149.1 testing for unlimited distance is possible using high-speed communication media.

Conclusions

- No longer a certainty that board boundary-scan access can only be achieved via the edge connector.
- Subsequently we should utilise any existing wired or wireless interface that the product design supports.
- The 'TapSpacer™' technology allows the use of existing communication channels using minimal hardware and no modifications to COTS test software.
- Inherent performance limitations can be overcome using a fast transmission media i.e. 1 Gbit Ethernet.
- Provides a simple one-for-all testability solution from 'cradle-to-grave'